IN THE CLAIMS:

Please amend claims 39-41 as follows.

1. (Previously Presented) A method, comprising:

determining, at a processor, a limiting signal from a signal filtered using a pulse shaping filter;

determining an error signal using the signal and the limiting signal by changing the limiting signal so as to be of an opposite sign and reducing from the signal; and

generating a limited signal by reducing an error signal filtered using a filter matched to a chip pulse waveform from the signal.

2. (Previously Presented) A method, comprising:

determining, at a processor, a limiting signal from a signal filtered using a pulse shaping filter;

determining an error signal using the signal and the limiting signal by changing the limiting signal so as to be of an opposite sign and reducing from the signal;

orthogonalizing the error signal filtered using a filter matched to a chip pulse waveform; and

generating a limited signal by reducing the orthogonalized error signal from the signal.

3. (Previously Presented) A method, comprising:

combining, at a processor, at least two signals modulated on different carriers to a combination signal;

determining a limiting signal from the combination signal filtered using a pulse shaping filter;

determining an error signal using the combination signal and the limiting signal by changing the limiting signal so as to be of an opposite sign and reducing from the signal;

dividing the error signal onto different carriers in a predetermined manner; and

generating limited signals by reducing each error signal part filtered using a filter matched to a chip pulse waveform from a corresponding signal.

4. (Previously Presented) The method as claimed in claim 1, wherein the signal is a baseband signal.

5. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is a baseband signal.

6. (Previously Presented) The method as claimed in claim 1, wherein the error signal is a baseband signal.

7. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is determined using a threshold value set for power or amplitude values.

8. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is determined using a threshold value set for power or amplitude values, the threshold value being set bearing in mind the maximum value predetermined for an error vector magnitude.

9. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is determined using a threshold value set for power or amplitude values, the threshold value being set bearing in mind the maximum value predetermined for a peak code domain error.

10. (Previously Presented) The method as claimed in claim 1, wherein the limiting signal is determined using a threshold value set for power or amplitude values, the threshold value being set so as to obtain the desired peak-to-mean ratio, peak-to-average ratio, crest factor of the power or amplitude.

11. (Previously Presented) The method as claimed in claim 2, wherein a clipping stage is added.

12. (Previously Presented) The method as claimed in claim 2, wherein orthogonalization is carried out by minimizing the equation

$$\left\| \begin{bmatrix} x_1 & x_2 & \cdots & x_p \end{bmatrix} \begin{bmatrix} c_{1,1} & c_{2,1} & \cdots & c_{n,1} \\ c_{1,2} & c_{2,2} & \ddots & c_{n,2} \\ \vdots & \vdots & \ddots & \vdots \\ c_{1,p} & c_{2,p} & \cdots & c_{n,p} \end{bmatrix} - \begin{bmatrix} y_1 & y_2 & \cdots & y_n \end{bmatrix} \right\|.$$

13. (Previously Presented) The method as claimed in claim 2, wherein the orthogonalizing the error signal utilizes unused codes.

14. (Previously Presented) The method as claimed in claim 2, wherein the orthogonalizing the error signal utilizes codes used at a lower modulation level.

15. (Previously Presented) The method as claimed in claim 3, wherein the dividing the error signal is carried out according to carriers.

16. (Previously Presented) The method as claimed in claim 3, wherein the error signal is divided equally between different carriers.

17. (Previously Presented) The method as claimed in claim 3, wherein the error signal is divided between different carriers in relation to power or amplitude values to be clipped.

18. (Previously Presented) An apparatus, comprising:

means for determining a limiting signal from a signal filtered using a pulse shaping filter;

means for determining an error signal using the signal and the limiting signal by changing the limiting signal so as to be of an opposite sign and reducing from the signal;

means for generating a limited signal by reducing the error signal filtered using a filter matched to a chip pulse waveform from the signal; and

means for filtering the limited signal using the pulse shaping filter.

19. (Previously Presented) An apparatus, comprising:

means for determining a first limiting signal from a signal filtered using a pulse shaping filter;

means for determining a first error signal using the signal and the first limiting signal;

means for orthogonalizing the first error signal filtered using a filter matched to a chip pulse waveform;

means for generating a first limited signal by reducing the orthogonalized first error signal from the signal;

means for determining a second limiting signal from the first limited signal filtered using the pulse shaping filter;

means for determining a second error signal using the first limited signal and the second limiting signal;

means for generating a second limited signal by reducing the second error signal filtered using a filter matched to a chip pulse waveform from the signal; and

means for filtering the second limited signal using the pulse shaping filter.

20. (Previously Presented) An apparatus, comprising:

means for combining at least two signals modulated on different carriers to a combination signal;

means for determining a limiting signal from the combination signal filtered using a pulse shaping filter;

means for determining an error signal using the combination signal and the limiting signal;

means for dividing the error signal onto different carriers in a predetermined manner;

means for generating limited signals by reducing each error signal part filtered using a filter matched to a chip pulse waveform from a corresponding signal;

means for filtering the limited signals using the pulse shaping filter; and

means for generating a combined limited signal by combining the filtered limited signals.

21. (Previously Presented) An apparatus, comprising:

means for filtering signals modulated on different carriers using pulse shaping filters;

means for combining at least two filtered signals to a combination signal;

means for determining a limiting signal from the combination signal;

means for determining an error signal using the combination signal and the limiting signal;

means for dividing the error signal onto different carriers in a predetermined manner;

means for generating limited signals by reducing each error signal part filtered using a filter matched to a chip pulse waveform from a corresponding signal;

means for filtering the limited signals using the pulse shaping filter; and

means for generating a combined limited signal by combining the filtered limited signals.

22. (Previously Presented) The apparatus as claimed in claim 35, wherein the signal is a baseband signal.

23. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting signal is a baseband signal.

24. (Previously Presented) The apparatus as claimed in claim 35, wherein the error signal is a baseband signal.

25. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting determiner is further configured to determine the limiting signal using a threshold value set for power or amplitude values.

26. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting determiner is further configured to determine the limiting signal using a threshold value set for power or amplitude values, the threshold value being set bearing in mind the maximum value predetermined for an error vector magnitude.

27. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting determiner is further configured to determine the limiting signal using a threshold value set for power or amplitude values, the threshold value being set bearing in mind the maximum value predetermined for a peak code domain error.

28. (Previously Presented) The apparatus as claimed in claim 35, wherein the limiting determiner is further configured to determine the limiting signal using a threshold value set for power or amplitude values, the threshold value being set so as to obtain the desired peak-to-mean ratio, peak-to-average ratio, crest factor of the power or amplitude.

29. (Previously Presented) The apparatus as claimed in claim 36, wherein the processor is further configured to carry out the orthogonalization of the first error signal according to carriers.

30. (Previously Presented) The apparatus as claimed in claim 37, wherein the divider is further configured to divide the error signal equally between different carriers.

31. (Previously Presented) The apparatus as claimed in claim 37, wherein the divider is further configured to divide the error signal between different carriers in relation to power or amplitude values to be clipped.

32. (Previously Presented) The apparatus as claimed in claim 36, wherein the processor is further configured to carry out orthogonalization by minimizing the equation

$$\left| \begin{bmatrix} x_1 & x_2 & \cdots & x_p \end{bmatrix} \begin{bmatrix} c_{1,1} & c_{2,1} & \cdots & c_{n,1} \\ c_{1,2} & c_{2,2} & \ddots & c_{n,2} \\ \vdots & \vdots & \ddots & \vdots \\ c_{1,p} & c_{2,p} & \cdots & c_{n,p} \end{bmatrix} - \begin{bmatrix} y_1 & y_2 & \cdots & y_n \end{bmatrix} \right|.$$

33. (Previously Presented) The apparatus as claimed in claim 36, wherein the processor is further configured to carry out orthogonalization utilizing unused codes.

34. (Previously Presented) The apparatus as claimed in claim 36, wherein the processor is further configured to carry out orthogonalization utilizing codes used at a lower modulation level.

35. (Previously Presented) An apparatus, comprising:

a limiting determiner configured to determine a limiting signal from a signal filtered using a pulse shaping filter;

an error determiner configured to determine an error signal using the signal and the limiting signal by changing the limiting signal so as to be of an opposite sign and reducing from the signal;

a generator configured to generate a limited signal by reducing the error signal filtered using a filter matched to a chip pulse waveform from the signal; and

a filter configured to filter the limited signal using the pulse shaping filter.

36. (Previously Presented) An apparatus, comprising:

a first limiting determiner configured to determine a first limiting signal from a signal filtered using a pulse shaping filter;

a first error determiner configured to determine a first error signal using the signal and the first limiting signal;

a processor configured to orthogonalize the first error signal filtered using a filter matched to a chip pulse waveform;

a first generator configured to generate a first limited signal by reducing the orthogonalized first error signal from the signal;

a second limiting determiner configured to determine a second limiting signal from the first limited signal filtered using the pulse shaping filter;

a second error determiner configured to determine a second error signal using the first limited signal and the second limiting signal;

a second generator configured to generate a second limited signal by reducing the second error signal filtered using a filter matched to a chip pulse waveform from the signal; and

a filter configured to filter the second limited signal using the pulse shaping filter.

37. (Previously Presented) An apparatus, comprising:

a combiner configured to combine at least two signals modulated on different carriers to a combination signal;

a limiting determiner configured to determine a limiting signal from the combination signal filtered using a pulse shaping filter;

an error determiner configured to determine an error signal using the combination signal and the limiting signal;

a divider configured to divide the error signal onto different carriers in a predetermined manner;

a first generator configured to generate limited signals by reducing each error signal part filtered using a filter matched to a chip pulse waveform from a corresponding signal;

a filter configured to filter the limited signals using the pulse shaping filter; and

a second generator configured to generate a combined limited signal by combining the filtered limited signals.

38. (Previously Presented) An apparatus, comprising:

a filter configured to filter signals modulated on different carriers using pulse shaping filters;

a combiner configured to combine at least two filtered signals to a combination signal;

a limiting determiner configured to determine a limiting signal from the combination signal;

an error determiner configured to determine an error signal using the combination signal and the limiting signal;

a divider configured to divide the error signal onto different carriers in a predetermined manner;

a first generator configured to generate limited signals by reducing each error signal part filtered using a filter matched to a chip pulse waveform from a corresponding signal;

a filter configured to filter the limited signals using the pulse shaping filter; and

a second generator configured to generate a combined limited signal by combining the filtered limited signals.

39. (Currently Amended) A non-transitory computer-readable medium encoded with a computer program, for controlling a processor to implement a method, the method comprising:

determining a limiting signal from a signal filtered using a pulse shaping filter;

determining an error signal using the signal and the limiting signal by changing the limiting signal so as to be of an opposite sign and reducing from the signal; and

generating a limited signal by reducing an error signal filtered using a filter matched to a chip pulse waveform from the signal.

40. (Currently Amended) A non-transitory computer-readable medium encoded with a computer program, for controlling a processor to implement a method, the method comprising:

determining a limiting signal from a signal filtered using a pulse shaping filter;

determining an error signal using the signal and the limiting signal by changing the limiting signal so as to be of an opposite sign and reducing from the signal;

orthogonalizing the error signal filtered using a filter matched to a chip pulse waveform; and

generating a limited signal by reducing the orthogonalized error signal from the signal.

41. (Currently Amended) A non-transitory computer-readable medium encoded with a computer program, for controlling a processor to implement a method, the method comprising:

combining at least two signals modulated on different carriers to a combination signal;

determining a limiting signal from the combination signal filtered using a pulse shaping filter;

determining an error signal using the combination signal and the limiting signal by changing the limiting signal so as to be of an opposite sign and reducing from the signal;

dividing the error signal onto different carriers in a predetermined manner; and

generating limited signals by reducing each error signal part filtered using a filter matched to a chip pulse waveform from a corresponding signal.